

### **AMENDMENTS TO THE SPECIFICATION**

Please replace paragraph [0003] with the following amended paragraph:

[0003] FIG. 1 shows the structure of a surface discharge type triode plasma display panel. FIG. 2 shows an example of a display cell of the plasma display panel shown in FIG. 1. Referring to FIGS. 1 and 2, address electrode lines  $A_{R1}$ ,  $[[A_{R2}]]$ ,  $A_{G1}$ ,  $\dots$ ,  $A_{Gm}$ ,  $A_{Bm}$ , dielectric layers 11 and 15, Y-electrode lines  $Y_1, \dots, Y_n$ , X-electrode lines  $X_1, \dots, X_n$ , phosphor layers 16, partition walls 17, and a magnesium oxide (MgO) layer 12 as a protective layer are provided between front and rear glass substrates 10 and 13 of a general surface discharge plasma display panel 1.

Please replace paragraph [0009] with the following amended paragraph:

[0009] Referring to FIGS. 4 and 5, in the typical driving apparatus using the address-display separation driving scheme as shown in FIG. 3, the X-driver 64 and the Y-driver 65 ~~works~~ work together. The X-driver 64 includes a single reset circuit  $RC_x$  and a single sustain circuit  $SC_x$ . The Y-driver includes a single reset/sustain circuit RSC and a single scan circuit.

Please replace paragraph [0020] with the following amended paragraph:

[0020] Accordingly, it can be inferred that a high power transistor for switching needs to be connected between an upper common power line  $PL_U$  of the upper transistors  $YU1$  through  $YUn$  of the switching output circuit SIC and the terminal of the scan bias voltage  $V_{SCAN}$ . When only a single high power transistor  $S_{SC1}$  or  $S_{SC2}$  is connected, the following problems occur.

Please replace paragraph [0021] with the following amended paragraph:

[0021] When only the second high power transistor  $S_{SC2}$  is connected, during the reset period and the display-sustain period, the driving signals  $O_{RS}$  of the reset/sustain circuit RSC are applied to the terminal of the scan bias voltage  $V_{SCAN}$  via an internal diode of the second high power transistor  $S_{SC2}$ , and thus a current flows. As a result, a driving operation during the reset period and the display-sustain period is unstable ~~instable~~ and requires high power consumption.

Please replace paragraph [0024] with the following amended paragraph:

[0024] In the meantime, when the third high power transistor  $S_{SP}$  is not connected and thus the upper common power line  $PL_U$  of the upper transistors  $YU1$  through  $YUn$  is merely disconnected with a lower common power line  $PL_L$  of the lower transistors  $YL1$  through  $YLn$ , during the reset period and the display-sustain period, the driving signals  $O_{RS}$  of the reset/sustain circuit RSC are applied to all of the Y-electrode lines  $Y_1$  through  $Y_n$  via all of the lower transistors  $YL1$  through  $YLn$  of the switching output circuit SIC and also applied to the first high power transistor  $S_{SC1}$  via internal diodes of the upper transistors  $YU1$  through  $YUn$  and an internal diode of the second high power transistor  $S_{SC2}$  of the scan driving circuit AC. As a result, the performance and the life span of the first high power transistor  $S_{SC1}$  are decreased. However, when the third high power transistor  $S_{SP}$  is connected, a voltage is dropped down by a predetermined level by the third high power transistor  $S_{SP}$  so that a voltage applied to the first high power transistor  $S_{SC1}$  can be decreased.

Please replace paragraph [0025] with the following amended paragraph:

[0025] In such a Y-driver of a typical driving apparatus, even when all of the lower transistors  $YL1$  through  $YLn$  of the switching output circuit SIC are turned off, the driving signals  $O_{RS}$  of the reset/sustain circuit RSC are applied to all of the Y-electrode lines  $Y_1$  through  $Y_n$  via

the lower common power line  $PL_L$  and the internal diodes of the upper transistors YU1 through YUn.

Please replace paragraph [0054] with the following amended paragraph:

[0054] The scan circuit of each of the first and second scan/sustain circuits SSC1 and SSC2 includes a scan driving circuit AC and a switching output circuit SIC and sequentially applies scan pulses to Y-electrode lines to perform an addressing operation of generating a predetermined wall voltage in selected display cells. The switching output circuit SIC includes upper transistors YU<sub>1</sub> through YU<sub>n/2</sub> and lower transistors YL<sub>1</sub> through YL<sub>n/2</sub> of an XY-electrode line pair group corresponding to the switching output circuit SIC, and common output lines of the respective upper and lower transistor pairs are connected to Y-electrode lines Y<sub>1</sub> through Y<sub>n/2</sub>, respectively. During an address period, the scan driving circuit AC generates driving signals to be applied to the Y-electrode lines Y<sub>1</sub> through Y<sub>n/2</sub> of the Y-electrode line pair group corresponding to the scan driving circuit AC. In other words, the scan driving circuit AC is connected to the an upper common power line PL<sub>U</sub> of the upper transistors YU<sub>1</sub> through YU<sub>n/2</sub> of the switching output circuit SIC and a lower common power line PL<sub>L</sub> of the lower transistors YL<sub>1</sub> through YL<sub>n/2</sub> of the switching output circuit SIC, applies a scan voltage to Y-electrode lines, which are scanned during the address period, and applies a scan bias voltage to Y-electrode lines, which are not scanned during the address period. FIG. 12 is a timing chart showing voltage waveforms of driving signals applied to electrode lines in a subfield when address-display mixing driving is performed by the driving apparatus shown in FIG. 6. In FIG. 12, a reference character O<sub>AR1 . . . ABm</sub> denotes a display data signal applied from the address driver 63 of FIG. 3 to the address electrode lines A<sub>R1</sub> through A<sub>Bm</sub> of FIG. 1. A reference character O<sub>x</sub> denotes a driving signal applied from the X-driver 64 of FIG. 3 to the X-electrode lines X<sub>1</sub> through X<sub>n</sub> of FIG. 1. A reference character O<sub>YG1</sub> denotes a driving signal applied from the first

scan/sustain circuit SSC1 to the Y-electrode lines  $Y_1$  through  $Y_{n/2}$  of the first XY-electrode line pair group. A reference character  $O_{YG2}$  denotes a driving signal applied from the second scan/sustain circuit SSC2 to the Y-electrode lines  $Y_{n/2+1}$  through  $Y_n$  of the second XY-electrode line pair group. A reference character R denotes a reset period. A reference character AM denotes a mixed period in which an address period and a mixed display-sustain period coexist. A reference character CS denotes a common display-sustain period. A reference character AS denotes a compensation display-sustain period.

Please replace paragraph [0058] with the following amended paragraph:

[0058] During the address period in the mixed period AM, a scan bias voltage  $V_{SC\_H}$  induced by charging a capacitor  $C_{SP}$  is applied to the upper common power line  $PL_U$  and the upper transistors  $YU_1$  through  $YU_{n/2}$  of the switching output circuit SIC. In addition, the high power transistor  $S_{SCL}$  is turned on. As a result, a negative scan voltage  $V_{SC}$  is applied to the lower transistors  $YL_1$  through  $YL_{n/2}$  of the switching output circuit SIC via the high power transistor  $S_{SCL}$ . Then, a lower transistor connected to a Y-electrode line to be scanned is turned on, and an upper transistor connected to the Y-electrode line to be scanned is turned off. In addition, lower transistors connected to all of other Y-electrode lines not to be scanned are turned off, and upper transistors connected to all of the other Y-electrode lines not to be scanned are turned on. Accordingly, the negative scan voltage  $V_{SC}$  is applied to the Y-electrode line to be scanned, and the scan bias voltage  $V_{SC\_H}$  is applied to the other Y-electrode lines not to be scanned.

Please replace paragraph [0066] with the following amended paragraph:

[0066] During the mixed display-sustain period in the mixed period AM, during the common display-sustain period CS, and during the compensation display-sustain period AS,

while the voltage of pulses applied to the Y-electrode lines  $Y_1$  through  $Y_{n/2}$  of the first XY-electrode line pair group increases from a ground voltage  $V_G$  to a second voltage  $V_S$ , only a first transistor ST1 is turned on. As a result, charges collected in an energy regeneration capacitor  $C_{SY}$  ~~[[is]]~~ are applied to the Y-electrode lines  $Y_1$  through  $Y_{n/2}$  of the first XY-electrode line pair group via inductor  $L_Y$ .

Please replace paragraph [0078] with the following amended paragraph:

[0078] During the mixed display-sustain period in the mixed period AM, during the common display-sustain period CS, and during the compensation display-sustain period AS, while the voltage of pulses applied to the X-electrode lines  $X_1$  through  $X_n$  increases from the ground voltage  $V_G$  to the second voltage  $V_S$ , only a 141st transistor ST141 is turned on. As a result, charges collected in an energy regeneration capacitor  $C_{SX}$  ~~[[is]]~~ are applied to the X-electrode lines  $X_1$  through  $X_n$  via an inductor  $L_X$ .